Air gaps for interconnects: ready to go?

Executive Overview

The scaling of the interconnect structure to smaller dimensions leads to an increase of the capacitance between metal lines. To offset this loss in performance (RC delay, cross-talk etc.), the IC industry has spent considerable effort on the development of dielectrics with lower k-value [1]. Initially, Si–O bonds were partially replaced with less polarizable bonds such as Si–F and Si–CH3 bonds. In order to realize further gains the porosity of the low–k dielectric was systematically increased. There are, however, boundaries to increasing porosity beyond 45–50% due to the percolation of pores. We describe several approaches that address this challenge.

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Because of the boundaries to increasing porosity, air gaps between metal lines yield performance gains that are unmatched by any low–k dielectric. In case of air gaps, the dielectric material is a sacrificial material, which is removed after the creation of the Cu wiring. Due to the increased number of process steps, the removal of the sacrificial material should be done in an economical way. Furthermore, it should not degrade the present Cu wires. And finally, it should not impose restrictions on the integration of further metal layers on top of the Cu/air gap level.

Integration approaches One integration approach aims at the creation of air gaps only in the areas of the metal level, where a capacitance decrease is needed. The remaining dielectric in the non–critical areas can thus provide mechanical support for the following metal levels. One variant of this approach for the selective removal of the dielectric can be realized by modifying the dielectric low–k surface after trench patterning such that the narrow dielectric spacings can be easily removed after the creation of the Cu wire by wet means, whereas the bulk of the dielectric remains intact [2].

While selective air gap formation provides good mechanical support, vias connecting the air gap level with the metal level above pose a reliability risk if they do not land completely on the Cu wire of the air gap level. To provide sufficient margin for unlanded vias, other approaches define areas using optical lithography in which the dielectric needs to be preserved in the air gap level around the via [3]. This approach was used to produce air gaps at various levels of the interconnect structure and good reliability performance was reported [4]. The mechanical stability of structures with air gaps on selected areas was measured by nano–indentation and nano–scratch, and it was found that the air gaps do not degrade the mechanical characteristics of interconnect structures [5].
In the approaches described above, the air gaps are created level per level. This increases the incremental cost with the number of air gap levels. Therefore, several approaches were developed, in which the sacrificial material is simultaneously removed from multiple air gap levels. This removal is realized by either evaporating the sacrificial material through a porous hard mask [6], by removing the sacrificial material via apertures [7], or by creating chimneys in non critical areas of the interconnect structure, which access several metal layers [8]. The sacrificial material can then be removed simultaneously through the chimneys from multiple levels via wet or dry etch. The removal of the sacrificial material through evaporation increases the thermal budget in the BEOL, which may impact not only the device performance, but also the k-value of low–k dielectric materials that may be used at other metal levels. The chimney approach can potentially reduce the cost of air gaps, while it also avoids issues such as unlanded vias or stress applied during CMP of metal levels on top of the air gap levels. Simultaneous air gap formation at multiple metal levels is therefore possible, and it addresses several air gap related issues (unlanded vias, mechanical stability, cost).

It is worth mentioning that the stress gradient of Cu wires will differ depending on the integration approach. It has been shown that the stress in a Cu wire is considerably lower when surrounded by air gaps, as opposed to an encapsulation with low–k or oxide [9]. If an area is defined underneath a via, where the dielectric is not removed (see the discussion above re: unlanded vias), a stress gradient will appear in the Cu wire at the transition between dielectric and air gap. The stress gradient may facilitate void formation in the Cu wire.

The various air gap technologies were mainly demonstrated in established technologies, i.e., in interconnect structures with a half–pitch of about 90–110nm. The need for air gap technologies is, however, predicted for significant smaller structures. For instance, the ITRS [10] indicates that a bulk k–value of 2.1–2.5 will be required for structures with a half–pitch of 28–36nm. Certainly for the lower range of the k–value, highly porous dielectrics will pose great challenges to integration due to plasma damage, which will inevitably lead to performance losses.

**Extrapolating results**

The question then arises how the performance and reliability results from the air gap technologies with rather relaxed dimensions can be extrapolated to the future technology nodes. To address this question, we have developed a single damascene test vehicle with a half–pitch of 35nm using double–patterning [11] and oxide as sacrificial material. The damascene integration process is the same as when creating Cu/oxide interconnects up to Cu CMP. After CMP, the sacrificial material is removed using wet etch, and the air gaps are then sealed by non–conformal deposition of a dielectric barrier. An example of the result is shown in the TEM of Fig. 1. A capacitance reduction of 50% was measured on air gaps formed by this approach, as compared to the oxide reference (Fig. 1).
There are a few advantages of the approach described above: scaling to smaller dimensions is facilitated by using SiO₂ for the damascene integration, which is a well known material that does not require particular etch or CMP development as it happens with porous low–k dielectric materials. Issues such as k–value increase due to plasma damage, post–etch polymer residues, Cu CMP on soft dielectrics or post–CMP cleaning are not a concern. In addition, the leakage current measured between Cu lines in the case of air gaps is almost one order of magnitude lower than in the case of oxide, as shown in Fig. 2. Since the CMP interface is removed during the wet etch of oxide, the dielectric failure of air gaps is not happening along the CMP interface anymore, as it has been found in many cases for low–k and oxide dielectrics. As a consequence, the dielectric reliability of air gaps can outperform that of non–air gap approaches, which can potentially be exploited both for memory and logic applications.
Figure 2. Comparison of the leakage current distribution of air gaps as compared to SiO₂.

References:


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Biographies

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